Figure 4 is a sectional view of Figure 3 along section lines 4'-4';

Figures 5a-5f, collectively referred to as Figure 5, are enlarged cross sectional views depicting one method of making a channel according to the present invention, using masking and etching to deposit a channel envelope onto a channel core;

Figures 6a-6h, collectively referred to as Figure 6, are enlarged cross sectional views depicting an alternative method of making at least one channel using a carrier wafer and a handle wafer;

Figures 7a-7f, collectively referred to as Figure 7, are enlarged cross sectional views depicting an alternative method of making a channel for a PFET using a shallow trench;

Figure 8a-f, collectively referred to as Figure 8, are perspective views of various embodiments of FinFET devices; and

Figure 9 depicts a SRAM circuit and is useful when discussing quantization.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

Figures 1 and 2a-2b are described above and serve as context for understanding the present invention. Figure 3 depicts in block diagram a FET 10. As known in the art, a source 12 and drain 14 are connected electrically via a channel 16, which is crossed by a gate 18. One or more channels 16 and gates 18 may be present in a single FET 10. As used herein, the length of the channel 16 is the distance from the source 12 to the drain 14 as depicted in Figure 3.

A sectional view of the channel 16 at section line 4'-4' is depicted at Figure 4. The FET 10 is disposed on a substrate 20 such as silicon 21 overlain with a layer of buried oxide 22. A channel core 24 is made from a first semiconductor material disposed over the substrate 20. The substrate 20 is preferably silicon based, such as a SIMOX wafer, a bonded wafer, or CZ silicon (silicon wafer from the Czochralski process) as known in the art. Preferably, the channel core 24 is formed atop the buried oxide layer 22 that forms